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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,195	02/20/2004	Mou-Shiung Lin	MS98-002CCC CIPB	6169
7590	10/28/2005		EXAMINER	
George O. Saile 28 Davis Avenue Poughkeepsie, NY 12603			LE, THAO X	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/783,195

Applicant(s)

LIN ET AL.

Examiner

Thao X. Le

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 October 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 94-129 and 131-135 is/are pending in the application.
- 4a) Of the above claim(s) 132-153 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 94-129 and 131 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Election/Restrictions*

1. Newly submitted claims 132-135 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

The newly submitted claims 132-135 and claims 94-131 are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because both the combination and subcombination are presented and assumed to be patentable, and it is evidence that the subcombination is patentable by itself and the combination does not require the gold layer or wirebonded. Furthermore, the subcombination has separate utility such as in the interconnection line or IC packaging. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 132-135 withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 95, 102, 107, 109, 126-127 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The specification discloses the insulating layer 4 in fig. 2 comprises oxide and nitride. But it fails to disclose TOPMOST nitride layer as claimed in claims 95, 107, and 126-127. Thus, they are indefinite. TOPMOST layer would have an exposed or no other layer over its surface.

For the purpose of examination, the insulation layer is being interpreted as comprises a nitride or oxide layer.

With respect to claim 102, there is no support of 'upper metallization structure is over topmast polymer layer. Thus, it is indefinite.

4. Claims 95, 97, 102, 107, 120, 126-128 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 95, 97, 107, 120, 127 and 128 recite the limitation "semiconductor chip or wafer". There is insufficient antecedent basis for this limitation in the claim. Assuming "semiconductor chip or wafer" is 'electronic component.

Claims 126 and 127 recite the limitation "insulating layer". There is insufficient antecedent basis for this limitation in the claims.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 94 and 120 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5436412 to Ahmad et al.

Regarding claim 94, Ahmad discloses an electronic component in fig. 2 comprising: a semiconductor substrate 10, col. 3 line 11, having multiple semiconductor devices, column 1 line 18, an interconnecting metallization structure 22/24, fig. 2, over said semiconductor substrate 10; an insulating layer 40, column 4 line 6, over said interconnecting metallization structure 22/24; and an upper metallization structure 34/44, column 4 line 4, over said insulating layer 40, wherein said upper metallization structure 34/44 comprises a metal layer, col. 4 line 36, having a thickness of between 3 and 5.0  $\mu\text{m}$ , col. 5 line 39, wherein said upper metallization structure 34/44 connects multiple portions 38 of said interconnecting metallization structure 22/24, fig. 2.

Layer 30 has the thickness of 3-5 $\mu\text{m}$ , col. 5 line 39; thus layer 34/44 would have at least 3-5 $\mu\text{m}$  in thickness.

Regarding claim 120, Ahmad discloses an electronic component comprising: a semiconductor substrate 10 having multiple semiconductor devices, fig. 2; an interconnecting metallization structure 22/24 over said semiconductor substrate 10 and comprising a contact point 38, a passivation layer 30 over said interconnecting

metallization structure 22/24, wherein said contact point 38 is exposed by an opening in said passivation layer 30; and a contact pad 34/44 connected to said contact point 38, wherein said contact pad 34/44 comprises a gold layer, col. 5 line 45, with a thickness of between 2 and 100  $\mu\text{m}$ .

Layer 44 is 1-2  $\mu\text{m}$  and layer 34 is 3-5  $\mu\text{m}$ ; total thickness of 34/44 is about 4-7 $\mu\text{m}$ .

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 94-105, 120-125, 128-129 and 131 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6417575 to Harada et al.

Regarding claims 94, 120, Harada discloses an electronic component in fig. 29-30 comprising: a semiconductor substrate 1, fig 30, having multiple semiconductor devices, fig. 1, an interconnecting metallization structure 250, column 25 line 2, over said semiconductor substrate 1; an insulating layer or passivation layer 15, column 24 line 23, over said interconnecting metallization structure 250; and an upper metallization structure 100, column 24 line 42, comprises gold, col. 19 line 47, over said insulating layer 15, wherein said upper metallization structure 100 comprises a metal layer having a thickness of between 1.5 and 3.0  $\mu\text{m}$ , col. 18 line 50, wherein said upper metallization

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structure 100 connects multiple portions of said interconnecting metallization structure 250, fig. 29.

The pad 100 further includes portion 251; thus the total thickness of the pad 100 would be exceeding 3.0  $\mu\text{m}$ .

Regarding claims 95-96, Harada discloses electronic component wherein said insulating layer 15 comprises a nitride layer 15c and oxide layer 15b, column 18 line 33-35f said electronic component.

Regarding claims 97,128, Harada discloses the electronic component of claim 94, wherein said insulating layer 15 comprises a CVD-formed layer, column 18 line 36.

Regarding claims 98-99, Harada discloses the electronic component of claim 94, wherein said interconnecting metallization structure 250 comprises a first contact pad (middle portion of 250) exposed by an opening in said insulating layer 15, and said upper metallization structure 100 comprises a second contact pad (right portion of 250) connected to said first contact pad, wherein the positions of said first and second contact pads from a top view are different, fig. 29 or 30, wherein said metal layer comprises gold, col. 19 lines 42-50.

Regarding claim 100-101,103, 105, 122, 124,129, Harada discloses the electronic component of claim 94, wherein said upper metallization structure further comprises an underlying metal layer 100a under said metal layer 100, wherein said underlying metal layer 100a comprises titanium or tungsten, col. 2 lines 38-45 and col. 3 line 10, wherein semiconductor substrate 1 comprises silicon, column 17 line 66

(semiconductor comprises silicon), wherein interconnecting metallization comprises electroplated copper, col. 3 line 15.

Regarding claim 102, 123, Harada discloses the electronic component of claim 94 further comprising a topmost polymer layer 203, column 24 line 59, over said insulating layer 15, wherein said upper metallization structure 100 comprises an upper metal layer 71 over said topmost polymer layer 70.

Regarding claim 104, 121, 125, Harada discloses the electronic structure of claim 94, wherein said interconnecting metallization structure comprises aluminum, column 19 lines 46.

Regarding claim 131, Harada discloses the electronic component further comprising a wirebonded 303 connected to contact pad 100, fig. 46.

### ***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation



under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 106-119 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5659201 to Wollesen.

Regarding claim 106, Wollesen discloses an electronic component in fig. 7-8 comprising: a semiconductor substrate 1, fig 1 column 1 line 53 and column 6 line 56, having multiple semiconductor devices, fig. 1, an interconnecting metallization structure 20/22/28, column 6 lines 52 and 55, over said semiconductor substrate 1 and comprising a first contact pad (right portion of 71), fig. 7; an insulating layer 23/24, fig. 7 column 6 lines 57-59, over said interconnecting metallization structure 20/22/28, wherein said first contact pad 72 is exposed by an opening in said insulating layer 23/24; and an upper metallization structure 71, column 8 line 22, over said insulating layer 24/24 and comprising gold, column 5 line 17, wherein said upper metallization structure 71 comprises a second contact pad (left portion of 71), fig. 7, connected to said first contact pad, and wherein the positions of said first and second contact pads from a top view are different, fig. 7.

But, Wollesen does not disclose the gold layer 71 having a thickness of between 2 and 100  $\mu\text{m}$ .

However, Wollesen discloses the gold layer 71 having a general thickness. Accordingly, it would have been obvious to one of ordinary skill in art

to use or combine (teaching of second reference) in the range as claimed, because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claims 107-108, Wollesen discloses the electronic component of claim 94, wherein said insulating layer 23/24 comprises a nitride layer 24, column 6 lines 59 and oxide layer 23, column 6 line 60, wherein insulating layer comprises a passivation layer 70, col.8 line 30.

Regarding claim 109-111, Wollesen discloses the electronic component wherein said insulating layer comprises said insulation layer 23/24, formed using a CVD process, column 6 line 47, wherein upper metallization structure further comprises a metal layer 73 under said gold layer 71 comprises Ti/W, col. 5 line 43, wherein said semiconductor substrate 1 comprises silicon, column 1 line 53 (semiconductor comprises silicon).

Regarding claim 112-115, Wollesen does not disclose the electronic component further comprising a wire bonded connected to said second contact pad, and further comprising a metal bump formed on said second contact pad.

However, Wollesen discloses in fig. 1 a second contact pad 14, column 2 line 14, comprising a wire bonded 15 connected to said second contact pad 14, and further comprising a metal bump (bottom portion of wire 15) formed on said second contact pad. At the time the invention was made; it would have been

obvious to one of ordinary skill in the art to use wire and metal bump teaching of Wollesen as claimed, because it would have allowed the external electrical connection.

Regarding claim 116, Wollesen discloses the electronic component further comprising a topmost polymer 70 layer over said insulating layer 23/24, wherein said upper metallization structure comprises an upper metal layer 71 over said topmost polymer layer 70.

Regarding claims 117, 119, Wollesen discloses the electronic component of claim 94, wherein said interconnecting metallization structure 20/22/28 comprises copper, column 6 line 61, wherein said upper metallization 71 structure comprises a metal, column 8 line 23.

The process limitations to 'electroplated copper' or 'electroplating' in claims 117 and 119 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claim 118, Wollesen discloses the electronic component of claim 94, wherein said interconnecting metallization structure 20/22/28 comprises aluminum, column 6 line 54.

### ***Response to Arguments***

12. Applicant's arguments filed 11 Oct. 2005 have been fully considered but they are not persuasive because

- a. Process limitation in the structure claim: even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In *re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), MPEP 2113. Furthermore, the Applicant argues that the 'electroplated copper or metal' is a structure limitation. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies on, i.e. lattice-orientation are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).
- b. With respect to the thickness of the bonding pad: since the applicant has not established the criticality of the thickness stated and since these the thickness are in common use in similar devices in the art, it would have been obvious to one of ordinary skill in the art to use these value in the device of thickness as claimed. Where patentability is said to be based upon particular chosen dimension or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In *re Woodruff*, 919 F2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

***Conclusion***

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

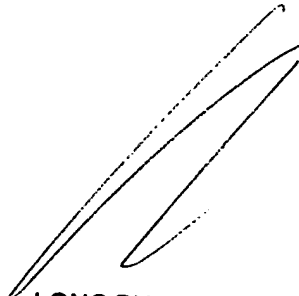
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le  
26 Oct. 2005



LONG PHAM  
PRIMARY EXAMINER